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Description

[SHALLOW TRENCH ISOLATION STRUCTURE AND DYNAMIC RANDOM ACCESS MEMORY, AND FABRICATING METHODS THEREOF]

Cross Reference to Related Applications

[0001] This application claims the priority benefit of Taiwan application serial no. 92113044, filed May 14, 2003.

Background of Invention

[0002] Field of the Invention

[0003] The present invention relates to structures of semiconductor devices and fabricating methods of the same. More particularly, the present invention relates to structures of shallow trench isolation (STI) and dynamic random access memory (DRAM), and fabricating methods of the same.

[0004] Description of the Related Art

[0005] With progressively increased functions of current com-

puter, the memory capacity required in any kind of computer is correspondingly getting larger and larger, and DRAM cells therefore need to be miniaturized continuously for further higher integration. In a deep sub-micron semiconductor process or a more advanced process, the lateral area for forming a DRAM cell and the accompanying storage capacitor is very small, and more sophisticated techniques are required to maintain the surface area of the storage capacitor for its storage capability.

[0006] Generally, the storage capacitors formed in DRAM can be divided into two categories according to their structures, namely, stacked capacitor and deep-trench capacitor. No matter which kind of capacitor structure is adopted, DRAM fabrication process gets more and more difficult as device dimensions are being decreased progressively.

[0007] On the other hand, in a fabrication process of a semiconductor device such as DRAM, an active area (AA) is usually defined and electrically isolated by forming a shallow trench isolation (STI) structure. When device dimensions are being decreased progressively, enhancing the isolation capability of STI structures is also an important issue.

[0008] There have been a variety of methods provided in the prior art for enhancing the isolation capability of STI

structures. For example, U.S. Publication No. 2002-0179997 discloses a method that forms a doped region, just after the shallow trench is formed, under the bottom of an STI layer to serve as a channel stop layer, thereby preventing a leakage current between two adjacent active areas.

[0009] However, when the doped region is formed under the bottom of an STI layer for enhancing the isolation capability of the STI layer, other leakage problems occur. For example, it is inevitable that some P-type ions are implanted into the sidewall of the shallow trench in the channel stop implantation process to form another doped region therein, since a back-scattering effect may let some ions be implanted into the sidewall of the shallow trench. The doped region in the sidewall of the shallow trench will overlap with the source/drain formed later, so that the junction gradient at the boundary of the source/drain is increased to cause a larger electric field, which further induces a junction leakage.

[0010] FIG. 1 illustrates a cross-sectional view of a conventional DRAM cell, which includes a trench capacitor 101 disposed in a substrate 100, an STI layer 122, an active device 136, a buried strap 110 coupling the active device

136 to the trench capacitor 101, an N-doped layer 126 and a P-doped layer 130. The trench capacitor 101 includes a lower electrode 102, an inter-electrode dielectric layer 104, an upper electrode 106 and a collar oxide layer 108 surrounding the upper portion of the upper electrode 106.

[0011] The N-doped layer 126 is formed to electrically connect the lower electrodes 102 of all trench capacitors 101 in the memory array (not shown). The P-doped layer 130 is formed in the substrate 100 at a depth just under the bottom of the STI layer 122, also traversing the channel region of a vertical parasitic transistor that consists of the buried strap 110, the lower electrode 102, the collar oxide layer 108 and the upper electrode 106. Therefore, the insulating capability of the STI layer 122 is improved, and the threshold voltage of the parasitic transistor is raised. If the threshold voltage of the parasitic transistor were not raised in this manner, the channel thereof would be turned on easily to cause a leakage of the charges on the capacitor and therefore lower the storage capability. The P-doped layer 130 is usually formed with a P-type ion implantation process after the STI layer 122 is formed.

[0012] Moreover, since the P-doped region 130 must be formed

at a depth just under the bottom of the STI layer 122 to effectively enhance the isolation capability, the P-doped layer 130 is formed close to the buried strap 110. Therefore, similar to the case mentioned above, the P-N junction gradient at the boundary of the buried strap 110 is increased, and a junction leakage is easily caused thereat.

SUMMARY OF INVENTION

[0013] In view of the foregoing, this invention provides a shallow trench isolation (STI) structure and a method for fabricating the same, wherein a doped region is formed under the bottom of the STI layer, and no doped region is formed in the sidewall of the shallow trench.

[0014] This invention also provides a DRAM structure and a method for fabricating the same capable of suppressing a leakage in a DRAM cell and improving the reliability of the memory device.

[0015] The method for fabricating a STI structure of this invention is described as follows. A patterned mask layer is formed on a substrate exposing a predetermined region for forming an STI layer, and then an ion implantation is performed using the mask layer as a mask to form a doped region in a predetermined depth within the substrate exposed by the mask layer. An etching process is

then conducted using the mask layer as a mask to etch the substrate down to the doped region and form a shallow trench. An insulating material is filled into the shallow trench, and then the mask layer is removed to complete the STI process.

[0016] The STI structure of this invention includes an STI layer and a doped region. The STI layer is disposed in a substrate, and the doped region is disposed in the substrate just under the bottom of the STI layer. Particularly, no doped region is formed in the sidewall of the shallow trench.

[0017] The method for fabricating a DRAM of this invention is described as follows. A trench capacitor is formed in a substrate, including a lower electrode, an inter-electrode dielectric layer and an upper electrode, and a buried strap is formed in the substrate connecting with the upper portion of the upper electrode. A patterned mask layer is formed on the substrate exposing a predetermined region for forming an STI layer, and then an ion implantation is performed using the mask layer as a mask to form a doped region of a first conductivity type in a predetermined depth within the substrate exposed by the mask layer. An etching process is then conducted using the

mask layer as a mask to etch the substrate down to the doped region and form a shallow trench. An insulating material is filled into the shallow trench, and then the mask layer is removed. Thereafter, a screen oxide layer is formed on the surface of the substrate, and then an ion implantation is performed to form a first doped layer of a second conductivity type in the substrate that electrically connects with the lower electrode of the trench capacitor. Another ion implantation process is conducted to form a second doped layer of the first conductivity type in the substrate at a depth between the doped region and the first doped layer. The screen oxide layer is removed, and an active device is formed on the substrate coupling with the trench capacitor via the buried strap.

[0018] The DRAM structure of this invention includes a trench capacitor, a buried strap, an STI layer, a doped region of a first conductivity type, a first doped layer of a second conductivity type, a second doped layer of the first conductivity type and an active device. The trench capacitor is disposed in a substrate, having a lower electrode, an inter-electrode dielectric layer and an upper electrode, and the buried strap is located in the substrate connecting with the upper portion of the upper electrode. The STI

layer is disposed in the substrate and has a portion encroaching upon the trench capacitor. The doped region of the first conductivity type is located in the substrate directly under the STI layer, the first doped layer in the substrate electrically connects with the lower electrode of the trench capacitor, and the second doped layer in the substrate is disposed at a depth between the doped region and the first doped layer. The active device is disposed on the substrate coupling with the trench capacitor via the buried strap.

[0019] As mentioned above, the method for fabricating a STI structure of this invention comprises, firstly, forming a doped region in a predetermined depth in the substrate as a channel stop layer, and then etching the substrate down to the doped region to form a shallow trench. Therefore, no implanted dopant exists in the sidewall of the shallow trench, and the P-N junction gradient at the boundary of the source/drain is not increased to cause junction leakage.

[0020] Moreover, since the doped region can serve as a detection end point in the etching process of the shallow trench, this invention has a better control over the depth of the shallow trench to improve the wafer to wafer trench depth

uniformity.

[0021] In addition, since the doped region as a channel stop layer is formed only under the bottom of the STI layer and no implanted dopant exist in the sidewall of the shallow trench in the DRAM cell of this invention, the P-N junction gradient at the boundary of the source/drain is not increased to cause a leakage of the charges on the storage capacitor.

[0022] Furthermore, since a doped region as a channel stop layer has been formed under the bottom of the STI layer, the second doped layer of the first conductivity type, e.g., a P-doped layer, can be formed in the substrate deeper than the doped region to be more distant from the buried strap. Therefore, the dopant concentration of the second doped layer can be increased as desired to raise the threshold voltage of the parasitic transistor as high as possible without increasing the P-N junction gradient to cause a leakage.

[0023] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0024] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0025] FIG. 1 illustrates a cross-sectional view of a conventional DRAM cell.

[0026] FIGs. 2A-2C illustrate a process flow of fabricating a STI structure according to a preferred embodiment of this invention in a cross-sectional view.

[0027] FIGs. 3A-3G illustrate a process flow of fabricating a DRAM cell according to a preferred embodiment of this invention in a cross-sectional view.

DETAILED DESCRIPTION

[0028] FIGs. 2A-2C illustrate a process flow of fabricating a STI structure according to the preferred embodiment of this invention in a cross-sectional view. At first, a patterned mask layer 204 is formed over a substrate 200 with a pad oxide layer 202 interposed between them for protecting the surface of the substrate 200. The mask layer 204 has a thickness larger than 600Å, for example, and can be a silicon nitride layer, a stacked silicon nitride/photoresist

layer or a stacked silicon nitride/silicon oxide/photoresist layer as required. The patterned pad oxide layer 202 and the patterned mask layer 204 are formed by, for example, sequentially forming a blanket oxide layer, a mask material layer and a patterned photoresist layer (not shown) on the substrate 200, and then etching the mask material layer and the blanket oxide layer using the patterned photoresist layer as a mask. If the photoresist layer is not removed after the etching step, it serves as a part of the patterned mask layer 204 mentioned above.

[0029] Thereafter, an ion implantation 206 is performed using the patterned mask layer 204 as a mask to form a doped region 208 in a predetermined depth within the substrate 200 exposed by the mask layer 204. The implanting energy of the ion implantation 206 is adjusted according to the depth of the shallow trench that will be formed later. For example, when an STI layer of 2900Åin thickness is to be formed in a 0.11□m process and boron ion is used in the implantation process, the implanting energy of boron ions is adjusted to around 100 KeV. In addition, the dopant in the doped region 208 can be a P-type dopant like boron or an N-type dopant, but has a conductivity type different from that of the active device formed later

to serve as a channel stop layer.

[0030] Referring to FIG. 2B, an etching process is performed using the mask layer 204 as a mask for etching the substrate 200 down to the doped region to form a shallow trench 210. The doped region 208 can serve as a detection end point of the etching process. Specifically speaking, when the dopants in the doped region are detected in the etching process, the etching process may be terminated according to the end point detection signal. Since the depth of the doped region 208 can be controlled precisely, the depth variation of the shallow trenches 210 between different wafers can be minimized to improve the wafer to wafer trench depth uniformity.

[0031] Referring to FIG. 2C, an insulating layer 212 is filled into the shallow trench 210, and then the mask layer 204 and the pad oxide layer 202 are removed to complete the STI process. The insulating layer 212 can be filled into the shallow trench 210 by, for example, blanket depositing an insulating material layer (not shown) over the substrate 200 covering the mask layer 204 and filling up the shallow trench 210, and then conducting a chemical mechanical polishing (CMP) process to polish the insulating material layer until the mask layer 204 is exposed.

[0032] Therefore, as shown in FIG. 2C, the STI structure of this invention is constituted of an STI layer 212 and a doped region 208. The STI layer 212 is disposed in a substrate 200, and the doped region 208 is located in the substrate 200 directly under the bottom of the STI layer 212. Particularly, no doped region is formed in the sidewall or the upper edge of the shallow trench 210.

[0033] The aforementioned STI structure can be applied to many kinds of semiconductor devices, such as DRAM. A DRAM structure having the STI structure and a fabricating method of the same are described below.

[0034] FIGs. 3A-3G illustrate a process flow of fabricating a DRAM cell according to the preferred embodiment of this invention in a cross-sectional view. A substrate 100, such as a P-type substrate, is provided, and then a trench capacitor 101 is formed in the substrate 100, including a doped region 102 as a lower electrode, an inter-electrode dielectric layer 104, a conductive layer 106 as an upper electrode and a collar oxide layer 108.

[0035] The trench capacitor 101 can be formed using the following steps. A deep trench, in which the conductive layer 106 will be formed later, is formed in the substrate 100, and then a doped region 102 is formed in the substrate

100 around the lower portion of the deep trench to serve as a lower electrode of the trench capacitor. An inter-electrode dielectric layer 104 is formed on the sidewall of the lower portion of the deep trench, and a collar oxide layer 108 is formed on the sidewall of the upper portion of the deep trench. Then, a conductive layer 106 is filled into the deep trench. Since some steps mentioned above are performed under high temperature conditions, the dopants in the conductive layer 106 diffuse into the substrate 100 from the interface not interposed by the collar oxide layer 108 to form a doped region 110, i.e., the buried strap 110.

[0036] After the fabrication of the trench capacitor 101 is completed, a patterned mask layer 302 is formed on the substrate 100 exposing a portion of the substrate 100 predetermined for forming a STI structure. In a preferred embodiment, the thickness of the mask layer 302 is larger than 600Å, and the mask layer 302 can be a silicon nitride layer, a stacked silicon nitride/photoresist layer or a stacked silicon nitride/silicon oxide/photoresist layer as required.

[0037] Referring to FIG. 3B, an ion implantation 304 is performed using the patterned mask layer 302 as a mask to form a

doped region 306 in a predetermined depth in the substrate 100 exposed by the mask layer 302. The implanting energy of the ion implantation 304 is adjusted according to the depth of the shallow trench that will be formed later. For example, when an STI layer of 2900Åin thickness is to be formed in a 0.11□m process and boron ion is used in the implantation process, the implanting energy of boron ions is adjusted to around 100 KeV. In addition, the dopant in the doped region 306 can be a P-type dopant like boron or an N-type dopant, but has a conductivity type different from that of the active device formed later to serve as a channel stop layer.

[0038] Referring to FIG. 3C, an etching process is performed using the mask layer 302 as a mask to form a shallow trench 308 down to the doped region 306 in the substrate 100. The shallow trench 308 encroaches upon a portion of the buried strap 110 and a top portion of the trench capacitor 101. The doped region 306 can serve as a detection end point of the etching process. Specifically speaking, when the dopants in the doped region 306 are detected in the etching process, the etching process may be terminated according to the end point detection signal. Since the depth of the doped region 306 can be controlled pre-

cisely, the depth variation of the shallow trenches 308 between different wafers can be minimized to improve the wafer to wafer trench depth uniformity.

[0039] Referring to FIG. 3D, an insulating layer 310 is filled into the shallow trench 308, and then the mask layer 302 is removed to complete the STI process. In a preferred embodiment, the insulating layer 310 can be filled into the shallow trench 308 by, for example, blanket depositing an insulating material layer (not shown) over the substrate 100 covering the mask layer 302 and filling up the shallow trench 308, and then conducting a chemical mechanical polishing (CMP) process to polish the insulating material layer until the mask layer 302 is exposed.

[0040] Referring to FIG. 3E, a screen oxide layer 312 is formed on the surface of the substrate 100 to prevent a channel effect in the subsequent ion implantation processes. An ion implantation 314 is conducted to form an N-doped layer 316 in the substrate 100 that electrically connects with the lower electrode 102 (doped region 102) of the trench capacitor 101. In fact, the N-doped layer 316 electrically connects with the lower electrodes of all trench capacitors in the memory array (not shown) to form a common electrode.

[0041] Referring to FIG. 3F, another ion implantation 318 is performed to form a P-doped layer 320 in the substrate 100 at a depth between the doped region 306 and the N-doped layer 316.

[0042] The P-doped layer 320 is formed to raise the threshold voltage of the vertical parasitic transistor that is constituted of the buried strap 110, the lower electrode 102, the collar oxide layer 108 and the upper electrode 106. If the threshold voltage of the parasitic transistor were not raised in this manner, the channel thereof would be turned on easily to cause a leakage of the charges on the trench capacitor 101 and therefore lower the storage capability. Moreover, since the doped region 306 as a channel stop layer has been formed under the bottom of the STI layer 310, the P-doped layer 320 can be formed in the substrate 100 deeper than the doped region 306 to be more distant from the buried strap 110. Therefore, the P-N junction gradient at the boundary of the buried strap 110 is not increased, and the junction leakage current can be suppressed. Furthermore, the dopant concentration of the P-doped layer 320 can be increased as required to further raise the threshold voltage and suppress the leakage of the vertical parasitic transistor more effectively.

[0043] Referring to FIG. 3G, the screen oxide layer 312 is removed after the above ion implantation processes. An active device 136 and a passing word line 138 are formed on the substrate 100, wherein the active device 136 includes a word line 132 and a source/drain 134a/134b, and is coupled to the buried strap 110 that electrically connects with the trench capacitor 101. That is, the active device 136 is coupled to the trench capacitor 101 via the buried strap 110.

[0044] Accordingly, as shown in FIG. 3G, the DRAM cell of this embodiment includes a trench capacitor 101, a buried strap 110, an STI layer 310, a P-doped region 306, a P-doped layer 320, an N-doped layer 316 and an active device 136. The trench capacitor 101 is disposed in the substrate 100, including a lower electrode 102, an inter-electrode dielectric layer 104 and an upper electrode 106. The buried strap 110 is located in the substrate 100 connecting with the top portion of the trench capacitor 101.

[0045] The STI layer 310 is disposed in the substrate 100, and has a portion encroaching upon the top portion of the trench capacitor 101. The P-doped region 306 is located in the substrate 100 directly under the STI layer 310.

[0046] The N-doped layer 316 is disposed in the substrate 100

electrically connecting with the lower electrode 102 of the trench capacitor 101. The P-doped layer 320 is disposed in the substrate 100 at a depth between the N-doped layer 316 and the P-doped region 306.

[0047] The active device 136 is disposed on the substrate 100, including a word line 132 and a source/drain 134a/134b. The active device 136 is coupled to the buried strap 110 that electrically connects with the trench capacitor 101. That is, the active device 136 is coupled to the trench capacitor 101 via the buried strap 110.

[0048] As mentioned above, the method for fabricating a STI structure of this invention comprises, firstly forming a doped region in a predetermined depth in the substrate as a channel stop layer, and then etching the substrate down to the doped region to form a shallow trench. Therefore, no implanted dopant exists in the sidewall of the shallow trench, and the P-N junction gradient at the boundary of the source/drain is not increased to cause a junction leakage.

[0049] Moreover, since the doped region can serve as an end-point indicator in the etching process of the shallow trench, this invention provides a better control over the depth of the shallow trench to improve the wafer to wafer

trench depth uniformity.

[0050] In addition, since the doped region as a channel stop layer is formed only under the bottom of the STI layer and no implanted dopant exists in the sidewall of the shallow trench in the DRAM cell of this invention, the P-N junction gradient at the boundary of the source/drain is not increased to cause a leakage of the charges on the storage capacitor.

[0051] Furthermore, since the doped region serving as a channel stop layer has been formed under the bottom of the STI layer, the second doped layer of the first conductivity type, e.g., a P-doped layer in the preferred embodiment, can be formed in the substrate deeper than the doped region to be more distant from the buried strap. Therefore, the dopant concentration of the second doped layer can be increased as desired to raise the threshold voltage of the parasitic transistor as high as possible without increasing the P-N junction gradient to cause a leakage.

[0052] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications

and variations of this invention provided they fall within the scope of the following claims and their equivalents.